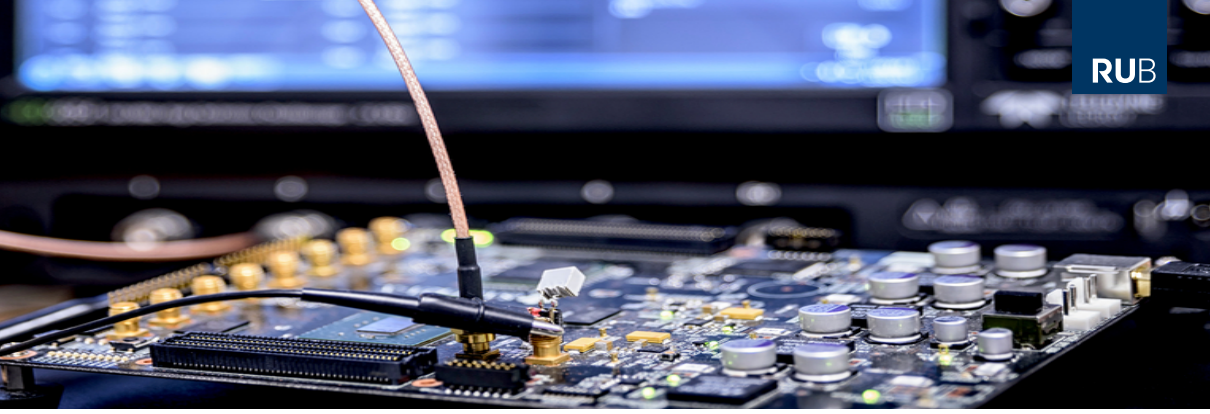

RUHR-UNIVERSITÄT BOCHUM

PQC in the Embedded World

Implementations, Side-Channel Attacks, and Countermeasures

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Chair for Security Engineering
Faculty of Computer Science
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June 28, 2022

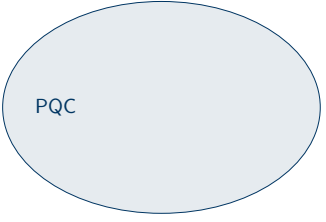
PROMETHEUS

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 780701.

What is PQC?

RUB

- PQC = any cryptography that withstands attacks from large-scale quantum computers
- basic (asymmetric) primitives: PKE/KEM and signatures
- advanced primitives: (F)HE, ZKP etc.
- this talk: PQC (only basic primitives) in the embedded world



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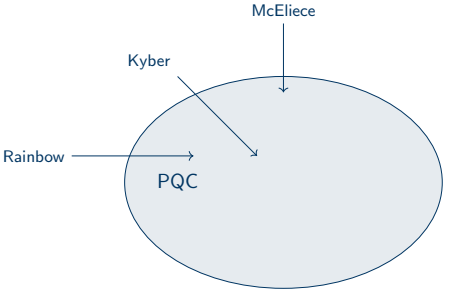

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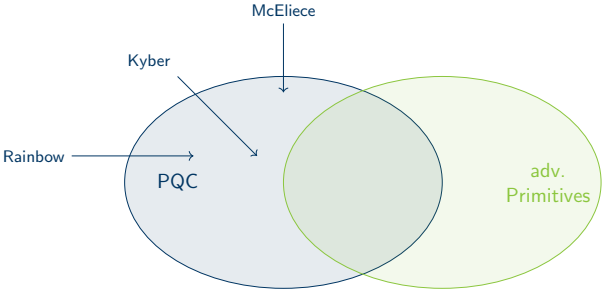

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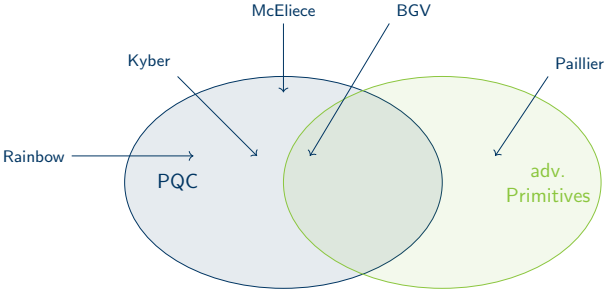

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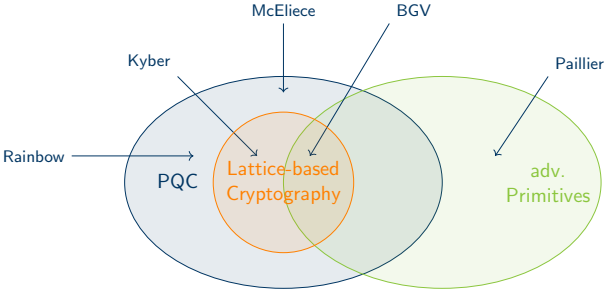

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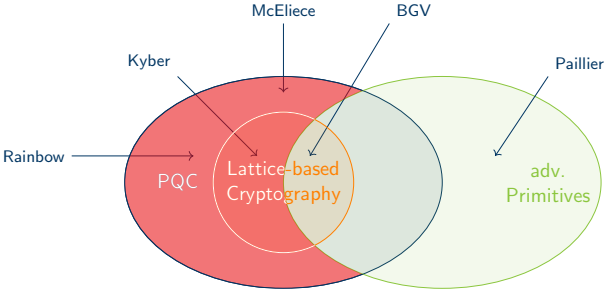

The Embedded World

not embedded

servers, laptops

embedded

smartcards, distributed sensor systems (IoT, cars, industry), ...

"Every computer that has no fan."

PQC and Embedded Systems: Requirements

RUB

small

- software: program memory and stack usage
- FPGAs: slices, LUTs, FFs, DSPs, BRAMs
- ASICs: area

fast

- latency
- throughput

secure

- passive side-channel attacks
- active side-channel attacks

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Embedded Software Implementations: KEMs

scheme	NIST security level	key gen (avg. kcycles)	encaps (avg. kcycles)	decaps (avg. kcycles)	program memory (kB)	key gen stack (kB)	encaps stack (kB)	decaps stack (kB)	ref.
ECDH	–	327	906		8.9		$\leq$2		[1]
Kyber	1	442	542	494	15	2.7	2.8	2.8	[2]
Saber	1	422	591	581	20	3.2	3.1	3.1	[2]
NTRU	1	2867	565	538	192	21	14	15	[2]
sNTRUp	1	6714	631	486	238	92	13	16	[2]
SIKE	1	48265	78911	84275	30	6	6	7	[2]
BIKE	1	65551	4963	116657	35	44	32	91	[2]
McEliece	1	1430811	582	2707	621	115	1.4	18	[3]

- Kyber and Saber are competitive to ECDH!
- NTRU variants may be used for use cases without key generation
- McEliece suitable for encaps-only use cases
- McEliece: lower memory footprint possible by streaming in the public key from a master device [4]

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Embedded Software Implementations: Signature Schemes

scheme	NIST security level	key gen (avg. kcycles)	sign (avg. kcycles)	verify (avg. kcycles)	program memory (kB)	key gen stack (kB)	sign stack (kB)	verify stack (kB)	ref.
ECDSA	–	327	375	976	8.9		≤2		[1]
Dilithium	2	1597	4095	1572	18	38	49	36	[2]
Falcon	1	162463	38999	474	121	1.4	2.6	0.4	[2]
Picnic	1	60	303854	203717	81	0.8	32	32	[2]
SPHINCS+	1	16112	400443	22548	4.5	2.1	2.2	2.7	[2]
XMSS	(1)	243255	247726	3207	–	4.0	4.0	3.8	[5]

- Falcon well-suited for verify-only use cases
- Dilithium has very balanced performance – verify can run with <8 kB [6]

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RUB

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Hardware Implementations: Targets

RUB

FPGA

- "field-programmable gate array"
- reconfigurable hardware
- area metrics: lookup tables, flip flops, DSPs, block RAM
- speed metrics: latency, throughput

ASIC

- "application-specific integrated circuit"
- not reconfigurable
- area metrics: area in mm^2
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SW / HW Codesign

- idea 1: new instructions for CPUs that speed up PQC schemes (instruction set extension)
- idea 2: whole co-processors
- proof of concept usually in FPGAs
- emerging: RISC-V is easily exensible

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Easy: Fast, but large area.

Easy: Small area, but slow.

The art: Low area-latency product.

Hardware Implementations: FPGA Implementations

- Kyber [7]
- Saber [8]
- McEliece [9]
- Dilithium [10–14]
- Falcon [13]
- Rainbow [15]
- BIKE [16, 17]
- sNTRU Prime [18, 19]
- ...

FPGA Implementations: BIKE

- first set of implementations: feasibility shown, already high speed and low area variant
- second set: vast improvements in both dimensions, additional mid-range core

LUTs	FFs	KeyGen μs	Encaps μs	Decaps μs	Ref.
13k	5354	21903	1252	13349	[16]
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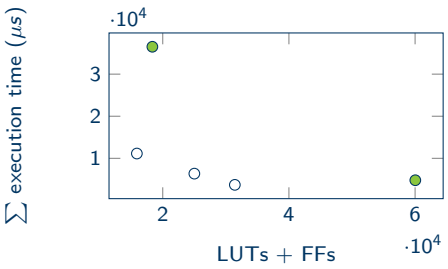

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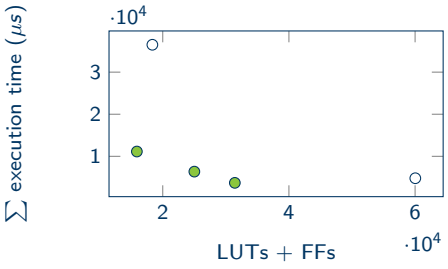

FPGA Implementations: Dilithium

RUB

- initial implementation [10] shows feasibility
- follow-up [11]: faster, supports all security levels
- novel idea [14]: run Saber and Dilithium with the same polynomial multiplier

LUTs	FFs	KeyGen μs	Sign μs	Verify μs	Ref.
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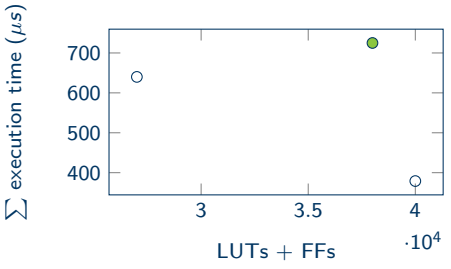

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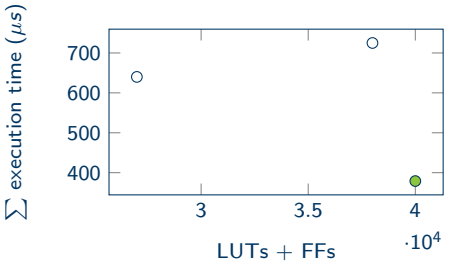

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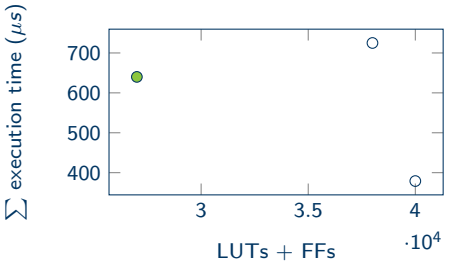

Hardware Implementations: ASICs and SW/HW Codesigns

ASICs

- only few implementations published: Kyber [20], Saber [21]
- FPGA implementations already good indicator of hardware cost

HW / SW Codesign

- RISC-V instruction set extensions for finite field arithmetic: low-level acceleration applicable to many schemes
- multiple works on this [22–24]
- biggest improvement would be: SHA-3 accelerator (some lattice-based schemes have up to 86% hashing, hash-based up to 95% [2])

Implementations

RUB

Don't sleep on these numbers, there is progress.

PQC and Side-Channel Attacks

RUB

devices everywhere

PQC and Side-Channel Attacks

devices everywhere, attackers everywhere

PQC and Side-Channel Attacks

devices everywhere, attackers everywhere

security?

PQC and Side-Channel Attacks: Attacker Models

secure scheme (under certain assumptions)

$$\neq$$

secure implementation!

Kyber is mathematically secure under certain assumptions, but there are side-channel attacks that find the secret key.

PQC and Side-Channel Attacks: Attacker Models

RUB

Has an attacker pyhsical access to the device?

No? Then we still need execution time independent from secret data.

Side-Channel Attacks

RUB

no physical access		
timing depends on secrets	$\Rightarrow$	measure execution time

physical access, passive		
processing a 1 drains more power / emanates more electromagnetic radiation than a 0	$\Rightarrow$	measure power / EM

physical access, active
induce a fault, learn information about the secret key from the output

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Side-Channel Attacks: Countermeasures

- CPU / hardware processes secrets
- attacker measures side-channel, finds out secrets
- hide secrets from CPU / hardware
- split secret into uniform random shares, perform computation on shares
- highly algorithm-specific!

Side-Channel Resistant Implementations

RUB

good: many schemes have masked SW implementations

Kyber [25, 26], Saber [27, 28], ...

Side-Channel Resistant Implementations

good: many schemes have masked SW implementations

Kyber [25, 26], Saber [27, 28], ...

bad: some of them are already broken again

Kyber [29], Saber [30]

Side-Channel Resistant Implementations

RUB

good: we already know some fault attacks

Kyber [31–33], Survey for lattice-based schemes [34]

Side-Channel Resistant Implementations

RUB

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Kyber [31–33], Survey for lattice-based schemes [34]

bad: for some, it is unclear how to prevent them efficiently

Side-Channel Resistant Implementations

bad: for some components, we do not yet know how to mask them

Gaussian sampling? fixed-weigth sampling?

Side-Channel Resistant Implementations

bad: for some components, we do not yet know how to mask them

Gaussian sampling? fixed-weigth sampling?

good: there is progress

masking polynomial inversion [35]

Side-Channel Resistant Implementations

bad: micro-architectural leakage often kills secure-proven gadgets

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bad: there are only few HW masked implementations

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more research necessary

Conclusion

Use cases must be planned carefully.

Memory – Bandwidth – Latency – Throughput – Attack Scenarios

Research just started in many fields.

It will narrow and intensify once there are standards.

Questions? Ideas? Suggestions?

Ask me, contact me: georg.land@rub.de

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